REMARKS

There are 19 claims pending, of which claims 1, 5, 8, 12, 15, 17, and 19 are in independent form. By this amendment, claims 3 and 8 have been amended to address antecedent concerns, claims 2, 4, 7, 9, 11, and 14 have been amended into independent form, and claim 19 has been amended to more particularly define the invention. Care has been exercised to avoid introduction of new matter.

Allowable Subject Matter

The Applicant thanks the Examiner for indicating that claims 15-18 are allowed and that claims 2, 4, 7, 9, 11, and 14 would be allowable if rewritten in a manner as set forth in item 12, page 6 of the outstanding Action. Accordingly, claims 2, 4, 7, 9, 11, and 14 have been amended into independent form.

Objection:

Claims 3 and 10 are objected to as lacking proper antecedent support.

In response, claims 3 and 10 have been amended to overcome this objection.

35 U.S.C. 102 Rejections:

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker et al.* (USPN 5,637,900, hereinafter "*Ker*").

For at least the reasons stated hereinbelow, this rejection is respectfully traversed.

It is extremely unclear in reviewing the outstanding Action which regions of ***Ker*b** are supposed to correspond to the specific turn-on retraining region as set forth in the

claim. Specifically, it is uncertain which "unnumbered" regions of Fig. 8 in ***Ker*** relate to the third and fourth regions as recited in claim 1. It is noted that the Office Action of December 3, 2001 had misinterpreted regions 630 and 720 as representing the third and fourth regions of claim 1. Particularly, the fourth region 720 as disclosed in Fig. 8 of ***Ker*** include N^+ and P^+ guard rings which prevent an injected substrate current from causing VDD-to-VSS latch-up (see col. 10, lines 44-48). As such, not only does ***Ker*** fail to teach or suggest any turn-on retraining region, it actually teaches an ESD protection device that enhances the turn-on behavior in the MOS transistor.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

For at least the reasons stated hereinbelow, this rejection is respectfully traversed.

The present invention, as set forth in claim 5, specifically requires that "the channel length of said first channel region is greater than the channel length of said second channel region to **reduce a turn-on speed of said first MOS transistor**" (Emphasis added).

On the other hand, the P2 MOS transistor 810 of ***Ker*** is a thick-oxide device (see col. 7, lines 1-3) and the P5 MOS transistor 820 of ***Ker*** is a thin-oxide MOS transistor (see col. 7, lines 14-16). Therefore, any difference in the gate lengths of the P2 and P5 MOS transistors as alluded to in the outstanding Action would not have any effect on reducing the turn-on speed of the first MOS transistor.

Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

It is also not clear in reviewing the outstanding Action which unnumbered regions disclosed in Fig. 8 of ***Ker*** relate to the P+ and N+ regions as set forth in the claim. However, it is clear that, unlike the claimed invention, there is simply no additional pick-up diffusion in ***Ker*** that surrounds the first MOS transistor so that the turn-on of the first MOS transistor is retrained.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

The present invention as set forth in claim 12 is characterized by, *inter alia*, a pair of first n^+ regions within a p-type substrate to define a first n-channel region for a first MOS transistor, a pair of second N^+ regions within the p-type substrate to define a second n-channel region for a second MOS transistor wherein the channel length of the first channel is greater than the channel length of the second channel.

By contrast, ***Ker*** discloses first P^+ regions 620/623 and second P^+ regions 640/650 within an n-type substrate as set forth in item 7 of the outstanding Action. As such, ***Ker*** simply cannot anticipate the present invention as set forth in claim 12 because it lacks at least the claimed elements with respect to the first and second N+ regions, especially in view of the incorrect designation of P^+ regions 620/623 and 650 of ***Ker*** as N+ regions by the outstanding Action.

Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

The present invention as now set forth in claim 19 requires at least one guarded device which is turned-on by a turn-on retrain means, wherein the ESD protection device can be turned-on before the guarded device is turned-on.

On the other hand, ***Ker*** discloses an ESD protection device that enhances the turn-on behavior rather than restraining the turn-on of the first MOS transistor (see col. 10, lines 44-48). Accordingly, not only does ***Ker*** fail to disclose any turn-on retrain means, it actually teaches away from such means as set forth in claim 19.

Claims 3, 6, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ker* in view of Admitted Prior Art, hereinafter "*APA*".

The ***APA*** does not compensate for the above-discussed deficiency in ***Ker***. Therefore, claims 3, 6, 10, and 13, which further recite features in the semiconductor structure as set forth in claims 1, 5, 8, and 12, are distinguishable over ***Ker*** and ***APA***, individually or in combination, for at least the reasons stated above with respect to claims 1, 5, 8, and 12.

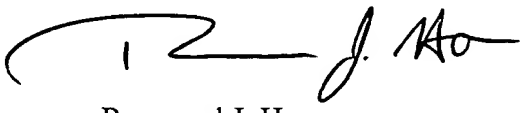
In view of the aforementioned accompanying remarks and amendments, claims 1-19 are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petitions for an appropriate extension of time. The fees for such an extension, or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-1299.

Respectfully submitted,

INTELLECTUAL PROPERTY SOLUTIONS, P.L.L.C.



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APPENDIX

(VERSION WITH MARKINGS TO SHOW CHANGES MADE)

IN THE CLAIMS:

2. (Twice Amended) [The semiconductor of claim 1,] A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type within said substrate for forming a drain of a first MOS transistor;

a second region of the second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate for forming a source of a second MOS transistor, wherein

a fourth region of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor, and

wherein the channel length of said first MOS transistor is longer than the channel length of said second MOS transistor to increase the drain-base voltage of said first MOS transistor.

3. (Amended) The semiconductor structure of claim 1, further comprising:

a pre-buffer circuit coupled to [said] a gate of the first MOS transistor; and

an output pad coupled to said first region of the first MOS transistor.

4. (Twice Amended) [The semiconductor structure of claim 1, further comprising:] A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type with said substrate for forming a drain of a first MOS transistor;

a second region of he second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate for forming a source of a second MOS transistor, wherein a fourth region of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor;

a first channel region disposed between said first and second regions of said first MOS transistor; and

a second channel region disposed adjacent to said third region of said second MOS transistor,

wherein said first channel length of said first channel region is longer than the channel length of said second channel region to increase the drain-base breakdown voltage of said first MOS transistor.

7. (Twice Amended) [The semiconductor structure of claim 5, further comprising] A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a pair of first regions of a second conductivity type within said substrate for defining a first channel region of the second conductivity type for a first MOS transistor;

a pair of second regions of the second conductivity type within said substrate for defining a second channel region of the second conductivity type for a second MOS transistor, wherein the channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn-on speed of said first MOS transistor; and

a third region of the first conductivity type between the source side of said first regions and the source side of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to further restrain the turn-on speed of said first MOS transistor.

9. (Twice Amended) [The semiconductor structure of claim 8,] A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate for forming a source of a second MOS transistor, wherein

a P+ region is disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on speed of said first MOS transistor, and

wherein the channel length of said first MOS transistor is longer than the channel length of said second MOS transistor to increase a drain-base breakdown voltage of said first MOS transistor.

10. (Amended) The semiconductor structure of claim 8, further comprising:

a pre-buffer circuit coupled to [said] a gate of the first MOS transistor; and

an output pad coupled to said first region of the first MOS transistor.

11. (Twice Amended) [The semiconductor structure of claim 8, further comprising:] A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate for forming a source of a second MOS transistor, wherein a P+ region is disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on speed of said first MOS transistor;

a first n-channel region having a first channel length and disposed between said first and second regions of said first MOS transistor; and

a second n-channel region having a second channel length disposed adjacent to said third region of said second MOS transistor,

wherein said first channel length is longer than said second channel length to further increase the drain-base breakdown voltage of said first MOS transistor.

14. (Twice Amended) [The semiconductor structure of claim 12, further comprising] A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate forming a base for said semiconductor structure;

a pair of first N+ regions within said substrate for defining a first n-channel region for a first MOS transistor;

a pair of second N+ regions within said substrate for defining a second n-channel region for a second MOS transistor, wherein the channel length of said first channel is greater than the channel length of said second channel; and

a third P+ region between the source region of said first N+ regions and the source region of said second N+ regions for surrounding said first MOS transistor with an additional pick-up diffusion to further restrain the turn-on of said first MOS transistor.

19. (Amended) A semiconductor structure for electrostatic discharge (ESD) protection comprising:

at least one ESD protection device; and

at least one guarded device which is turned-on by a turn-on restrained means,

wherein the ESD protection device can be turned-on before the [guarded device] turn-on restrained means is turned-on.